UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,303	12/03/2001	Sung-Chan Park	08244.0032	4821

7590 07/31/2002

Finnegan, Henderson, Farabow,
Garrett & Dunner, L.L.P.
1300 I Street, N.W.
Washington, DC 20005-3315

EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/31/2002

5

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/998,303	Applicant(s) PARK ET AL.	
	Examiner Thanh T. Nguyen	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following informalities or oversight: In the step © the antecedent basis of "conductive layer patterns" is not clear because "at least one" conductive layer pattern in step (a) can be one conductive layer pattern or more than one conductive layer patterns. Change to "forming conductive layer patterns on a substrate" in step (a) is suggested.

Claims 6 and 16 are objected because of the following informality or typo or oversight: it is unclear that how forming a mask pattern covering a top portion of the conductive layer can be formed after an interlayer insulating layer. In order to avoid the confusion, the following claim language is suggested: In line 1 of claims 6 and 16, respectively, change "after step b" to "after step a" is suggested.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8 and 18 include improper Markush terminology because the scope of Markush-type claims must be ascertainable, it cannot be open. Change "a gas selected from Ar,....." to "a gas selected from a group consisting of Ar,....." is suggested.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-3 and 11-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Duane et al. (U.S. Patent No. 6,329,695).

Referring to figures 11-15 (as claimed in claims 1-3), Duane et al. teaches an embodiment of a method of forming a semiconductor device comprising the steps of:

forming at least one conductive layer pattern (46, 48, 50) on a substrate (40), thereby forming a resulting structure (see figure 11 and col. 9, lines 30-38),

removing upper portion of layer (60) to form interlayer insulating layer (76 and 78), material for layer (60) is silicon oxide, silicon nitride, silicon oxynitride or low dielectric constant material of less than 3.5 (see col. 7, lines 64-67 and col. 8, lines 1-18, as required in claims 2-3) on the resulting structure (see figure 11),

exposing contact regions (56) (see figure 13) between the conductive layer patterns (46, 48) by etching the interlayer insulating layer (78),

after above step, forming an insulating spacer (84, formed from layer 82) on the sidewalls of the conductive layer patterns (46, 48, 50) (see figures 14-15).

Referring to figures 3-7 (as claimed in claims 11-13), Duane et al. teaches another embodiment of a method of forming a semiconductor device comprising the steps of:

forming at least one conductive layer pattern (46, 48, 50) on a substrate (40), thereby forming a resulting structure (see figure 2 and col. 7, lines 18-49),

forming an interlayer insulating layer (60, such as silicon oxide, silicon nitride silicon oxynitride or low dielectric constant material of less than 3.5; see col. 7, lines 64-67 and col. 8, lines 1-18, as required in claims 12-13) on the resulting structure (see figure 6),

exposing contact regions (56) (see figure 7) between the conductive layer patterns (46, 48, 50) by etching the interlayer insulating layer (60), and at the same time, forming an insulating spacer (64) by leaving the interlayer insulating layer (60) on the sidewalls of the conductive layer patterns (46, 48, 50) (see figures 6-7).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 11, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Cooper et al. (U.S. Patent No. 5,219,793).

Referring to figures 1-12, Cooper et al. teaches a method of forming a semiconductor device comprising the steps of:

forming at least one conductive layer pattern (14) on a substrate (12), thereby forming a resulting structure (see figure 1),

forming an interlayer insulating layer (18, glass, oxide, TEOS, or the like; see col. 3, lines 65-68) on the resulting structure (see figure 1),

exposing contact regions (see figure 5) between the conductive layer patterns (14) by etching the interlayer insulating layer (18), and at the same time, forming an insulating spacer (26) by leaving the interlayer insulating layer (18) on the sidewalls of the conductive layer patterns (14) (see figures 3-5).

Regarding to claim 16, due to the indefinite the limitation: after step a) forming a mask pattern (16) covering a top portion of the conductive layer pattern (14) wherein the mask pattern (16) is formed of a layer selected from a group consisting of silicon nitride (read on figure 1, col. 3, lines 56-63).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6, 8-10, 14-16, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duane et al. (U.S. Patent No. 6,329,695) as applied to claims 1–3 and 11-13 above, and further in view of cooper et al. (U.S. Patent No. 5,219,793).

Regarding to claims 4, 8, 14 and 18, the interlayer insulating layer is etched a gas mixture of CF_4, CHF_3, and argon (Ar) or using a gas selected from Ar, O_2, N_2, H_2, CH_4, C_2H_4 and C_xF_y. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Cooper et al.. Cooper teaches forming an oxide interlayer insulating layer (18) and SOG layer (22, spin on glass) is etched with a mixture of CF_4, CHF_3, and argon (Ar) or one of Ar, O_2 and C_2F_6, at the pressure of 150-350 mtorr (see col. 5, lines 4-19). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have used a mixture of CF_4, CHF_3, and argon (Ar) or one of Ar, O_2 and C_2F_6 to etch the interlayer insulating layer in Duane et al.'s process as taught by Cooper et al. ***because*** carbon and fluorine compound plasma can selectively etch the oxide interlayer insulating layer and remove all the oxide interlayer layer to expose the contact region between conductive patterns, and in the case when some spacing between conductive patterns wider than the other, the carbon and fluorine compound plasma can selectively etch the oxide interlayer insulating layer and leave a portion of oxide interlayer insulating layer on the sidewall of the conductive patterns to form sidewall spacers and also expose the contact region between the conductive patterns.

Regarding to claims 6, and 16 of forming a mask pattern covering a top portion of the conductive layer pattern wherein the mask pattern is formed of a layer selected from a group

consisting of silicon nitride. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Cooper. Cooper teaches forming a mask pattern (16) covering a top portion of the conductive layer pattern (14) wherein the mask pattern (16) is formed of a layer selected from a group consisting of silicon nitride (see figure 1 and col. 3, lines 52-63). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have formed a silicon nitride mask pattern covering a top portion of the conductive layer pattern in Duane et al.'s process as taught by Cooper et al. ***because*** the silicon nitride mask pattern provides protection to the top surface of conductive layer pattern during the etching process of interlayer insulating layer, so that the top surface of the conductive layer pattern can not be etched or damaged by the chemical or plasma.

Regarding to claims 5, 9, 15 and 19, the specific etching pressure range as claimed are taken to be obvious since these are variables of art recognized importance which are subject to routine experimentation and optimization and discovery of an optimum value for a known process is obvious. In re Aller, 105 USPQ 233 (CCPA 1955). And, even if applicants' modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art, In Re Sola 25 USPQ 433. Since, Cooper teaches that the oxide interlayer insulating layer (18, 22) is etched with a mixture of CF_4, CHF_3, and argon (Ar) or one of Ar, O_2 and C_2F_6 at the pressure of 150-350 mtorr (see col. 5, lines 4-19), hence, one of ordinary skill in the requisite art at the time the invention was made would have adjusted the plasma etching pressure to the range of less than 100 mtorr to etch the interlayer insulating layer ***because*** when an optimum etching pressure in

the etching chamber is used to etch the interlayer insulating layer, the interlayer insulating layer in the contact region can be completely removed or at the same time leaving a portion of the interlayer insulating layer on the sidewall of conductive layer patterns depending on the spacing between the conductive layer patterns.

Regarding to claims 10 and 20 of forming an etching mask having a contact hole pattern of straight-line shape. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Cooper. Cooper teaches forming an etching mask 24 having a contact hole pattern (23) of straight-line shape (see figure 2 and col. 4, lines 38-50). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have formed a completely straight line contact hole pattern in an etching mask covering a top portion of the conductive layer pattern in Duane et al.'s process as taught by Cooper et al. ***because*** the completely straight line contact hole pattern in the masking layer would ensure that the etching chemical or plasma follows the straight line shape of contact hole pattern to etch the interlayer insulating layer so that a smooth contact hole sidewall is formed in the interlayer insulating layer without forming undercut which traps contaminants and causing electrical current leakage.

Claims 7-8 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duane et al. (U.S. Patent No. 6,329,695) as applied to claims 1–3 and 11-13 above, and further in view of Chang et al. (U.S. Patent No. 6,159,842) and further in view of Tsai et al. (U.S. Patent No. 6,331,480).

Regarding to claims 7 and 17, the interlayer insulating layer is formed of a polymer. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Chang et al. Chang et al. teaches forming a low dielectric constant material layer HSQ layer (18) having a dielectric constant about 3 over the conductive layer patterns (14) (see figure 1 and col. 4, lines 22-40). The HSQ layer is a silicon polymer and spin-on insulating oxide material having a dielectric constant of 2.7-3.0 (see col. 1, lines 50-55). It would have been obvious to a person of ordinary skill in the art at the time of the invention was made would have used a silicon polymer HSQ layer having low dielectric constant to replace Duane et al.'s low dielectric interlayer insulating layer as taught by Chang et al. ***because*** silicon polymer HSQ layer can be easily deposited over the conductive layer patterns by spin-on coating process, and HSQ material also has the same low dielectric constant characteristics as the other low dielectric constant material which eliminates the capacitive interaction or coupling between closely-spaced conductive layer patterns.

Regarding to claims 8 and 18, the interlayer insulating layer is formed of a polymer and etched with a gas selected from Ar, O_2, N_2, H_2, CH_4, C_2H_4 and C_xF_y. Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Tsai et al. Tsai et al. teaches etching low dielectric constant material HSQ having a dielectric constant of about 2.5-3.5 with an etchant of O_2/C_2F_6 (see col. 3, lines 15-21).

Since, Chang et al. teaches forming a low dielectric constant material layer of polymer HSQ layer over the conductive layer patterns having a dielectric constant of 2.7-3.0. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made

would have etched a silicon polymer HSQ layer with an etchant of O_2/C_2F_6 in Chang et al.'s process as taught by Tsai et al. ***because*** Chang et al. and Tsai et al. both have similar HSQ material, and HSQ material layer which can be selectively etched with O_2 and/or C_2F_6 to form spacers on the sidewall of conductive layer pattern and/or expose the conductive region.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (703) 308-9439, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 7:00AM to 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN
July 16, 2002